WHAT IS CLAIMED IS:

1. A method of in circuit emulation of an integrated circuit including a digital data processor capable of executing program instructions, comprising the steps of:

detecting a first debug event during normal program execution;

upon detection of the first debug event suspending program execution except for at least one type interrupt service routine executed in response to a corresponding interrupt;

incrementing a debug frame counter upon each interrupt;

decrementing the debug frame counter upon each return from interrupt; and

detecting at least one second debug event during an interrupt service routine;

upon detection of the second debug event suspending program execution of the interrupt service routine while permitting execution of other interrupt service routines in response to corresponding interrupts; and

storing the count of said debug frame counter upon each second debug event.

2. The method of claim 1, wherein said integrated circuit includes a plurality of debug event detectors, and wherein:

said step of detecting a first debug event occurs at a first one of the plurality of debug event detectors;

said step of detecting a second debug event occurs at a second one of the plurality of debug event detectors; and

said step of storing the count of said debug frame counter occurs at said second one of the plurality of debug event detectors.

3. The method of claim 2, further comprising:

determining an order of interrupts triggering second debug events by reading said stored count of said debug frame counter from each of said debug event detectors.